

N-Channel Enhancement Mode MOSFET

TDM31090

DESCRIPTION

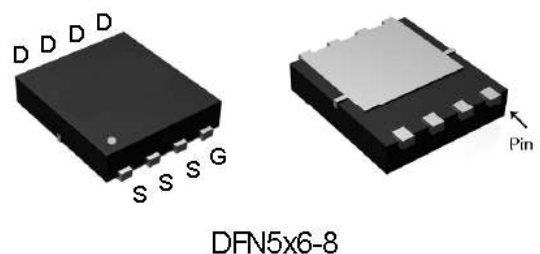
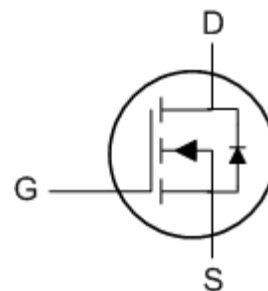
The TDM31090 is the high cell density trenched Nch MOSFETs, which provide excellent RDS(ON) and gate charge for most of the Synchronous Rectification for AC/DC Quick Charger.

GENERAL FEATURES

- RDS(ON) < 8mΩ @ VGS=10V
RDS(ON) < 10.5mΩ @ VGS=4.5V
- High Power and current handling capability
- Lead free product is available
- Surface Mount Package

Application

- PWM applications
- Load switch
- DC/DC in Telecoms and Industrial
- Hard Switched and High Frequency Circuits



ABSOLUTE MAXIMUM RATINGS(T_A=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	±20	V
Drain Current @ Continuous	I _D (T _C =25°C) Note1,5	74	A
	I _D (T _C =100°C) Note1,5	47	A
Pulsed Drain Current	I _{DM} Note2	260	A
Avalanche Current, Single pulse	I _{AS} Note2	31	A
Avalanche Energy, Single pulse	E _{AS} Note3	240	mJ
Thermal Resistance,Junction-to-Case	R _{θJC}	1.5	°C/W
Thermal Resistance,Junction-to-Ambient	R _{θJA} Note1	50	°C/W
Total Power Dissipation	P _D (T _C =25°C) Note4	83	W
Maximum Operating Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55 To 150	°C

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.4	1.7	2.4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$	-	6.5	8	m Ω
	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=10A$	-	8.8	10.5	m Ω
Forward Transconductance	G_{fs}	$V_{DS}=5V, I_D=10A$	-	60	-	S
Gate Resistance	R_G	$V_{GS}=0V, V_{DS}$ Open, $f=1\text{MHz}$	-	1.3	-	Ω
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V, F=1.0\text{MHz}$	-	1876	-	PF
Output Capacitance	C_{oss}		-	348	-	PF
Reverse Transfer Capacitance	C_{rss}		-	5.6	-	PF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, V_{GS}=10V, R_G=10\Omega, I_D=20A$	-	7	-	nS
Turn-on Rise Time	t_r		-	4	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	20	-	nS
Turn-Off Fall Time	t_f		-	3	-	nS
Total Gate Charge	Q_g	$V_{DS}=50V, I_D=20A, V_{GS}=4.5V$	-	16	-	nC
Total Gate Charge	Q_g	$V_{DS}=50V, I_D=20A, V_{GS}=10V$	-	32	-	nC
Gate-Source Charge	Q_{gs}		-	6	-	nC
Gate-Drain Charge	Q_{gd}		-	4	-	nC
Body Diode Reverse Recovery Time	T_{rr}		$I_F=20A, di/dt=500A/\mu s$	-	40	-
Body Diode Reverse Recovery Charge	Q_{rr}	-		160	-	nC
Diode Forward Voltage (Note 2)	V_{SD}	$V_{GS}=0V, I_S=1A$	-	-	1.2	V

NOTES:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width $\cong 300\mu s$, duty cycle $\cong 2\%$
3. The EAS data shows Max. rating. The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.3mH, I_{AS}=35A$
4. The power dissipation is limited by junction temperature
5. The maximum current rating is package limited.

Typical Operating Characteristics

Fig 1. Typical Output Characteristics

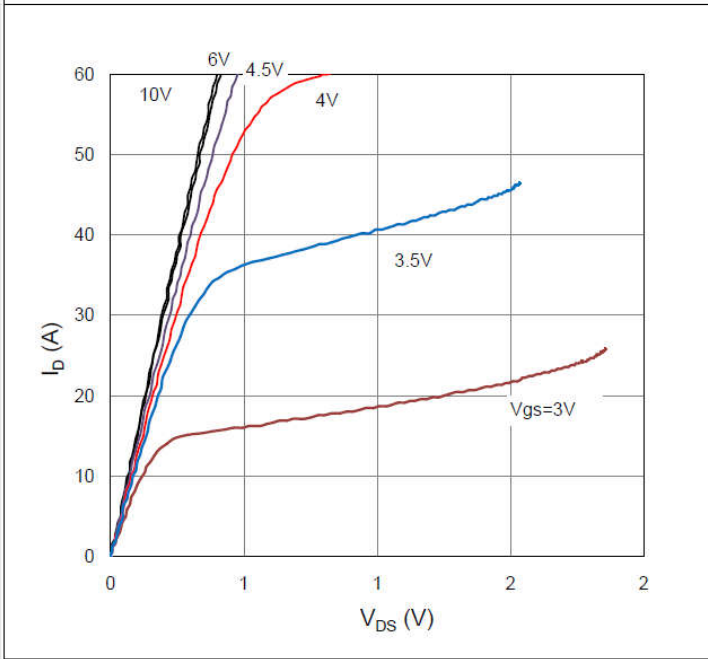


Figure 2. On-Resistance vs. Gate-Source Voltage

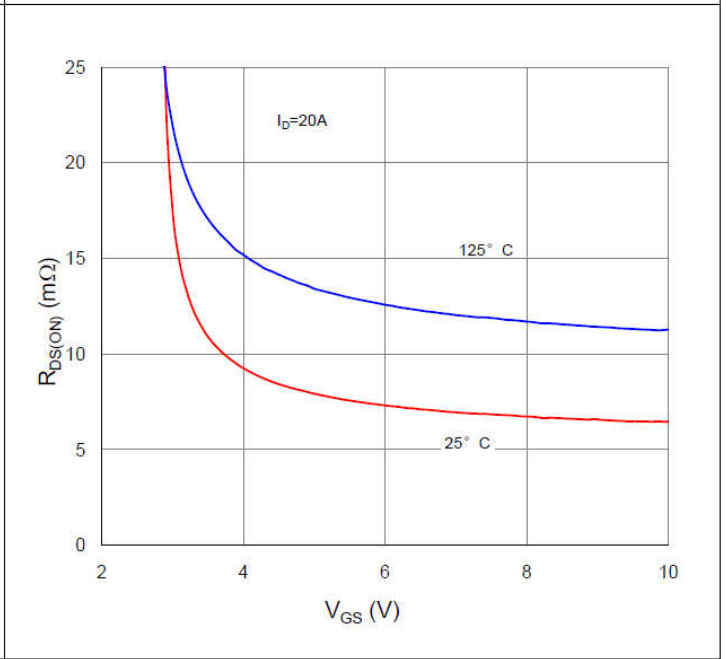


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

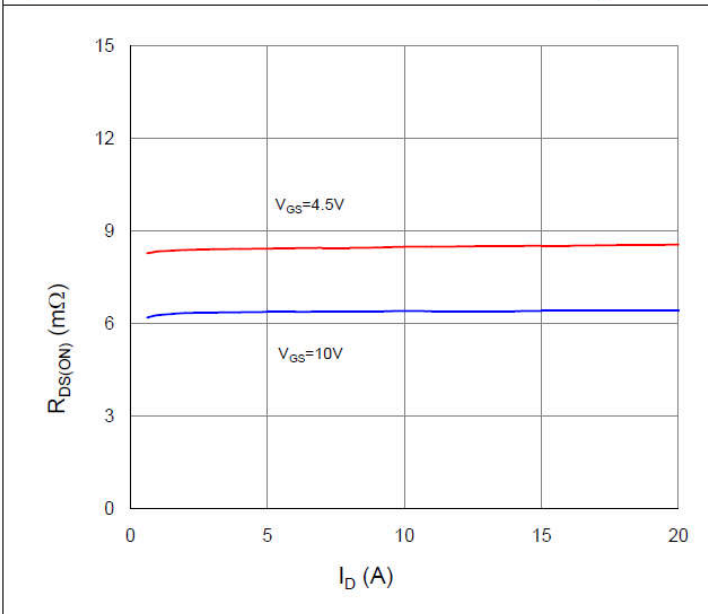
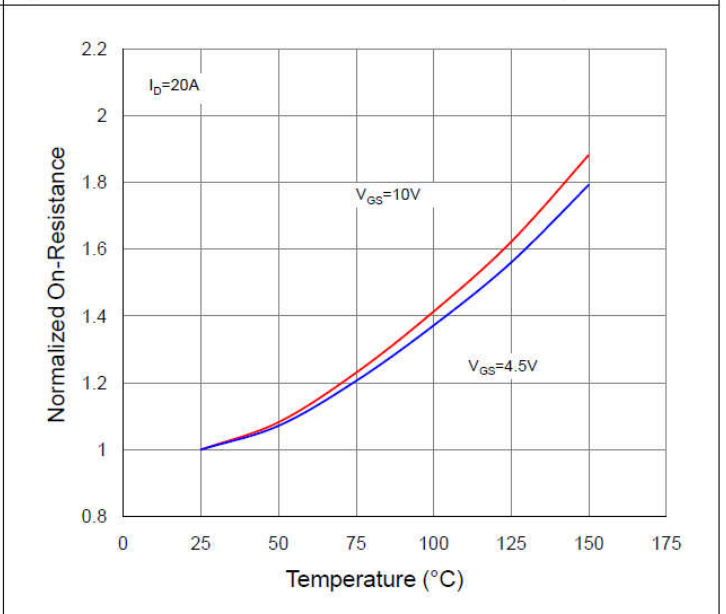


Figure 4. Normalized On-Resistance vs. Junction Temperature



Typical Operating Characteristics (Cont.)

Figure 5. Typical Transfer Characteristics

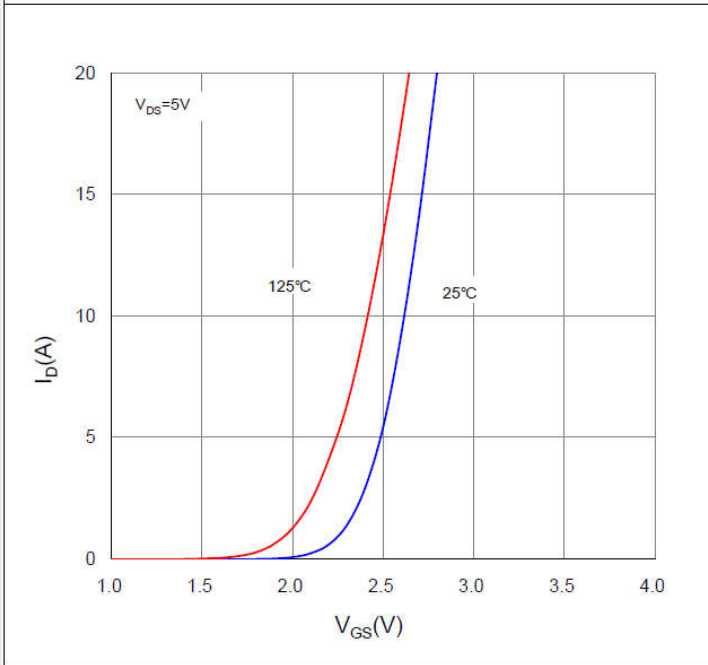


Figure 6. Typical Source-Drain Diode Forward Voltage

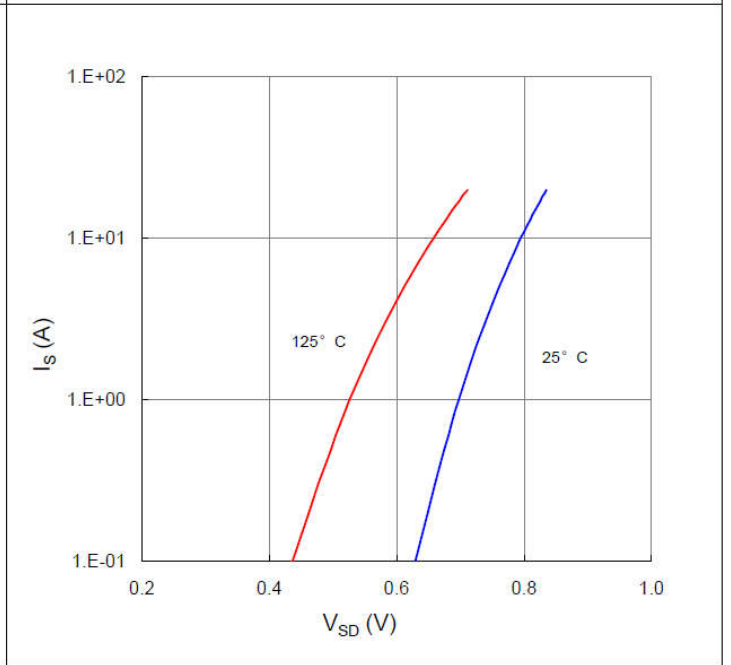


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

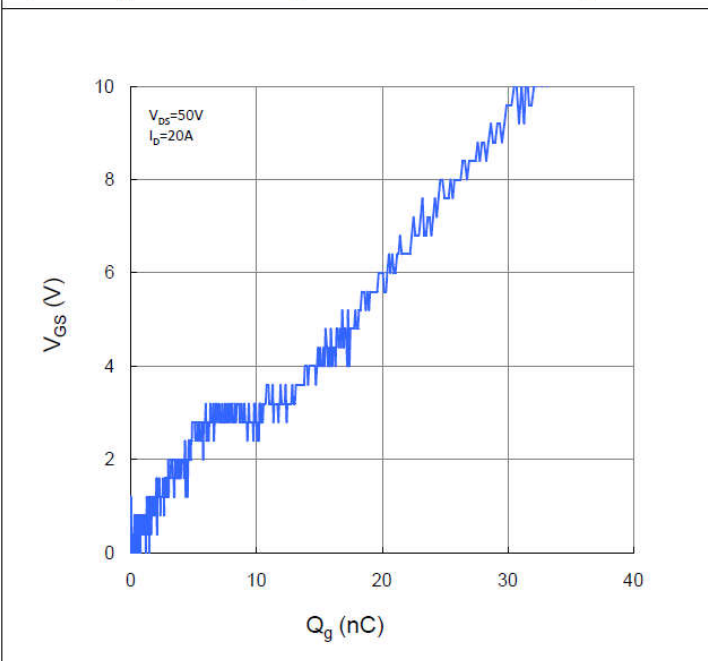
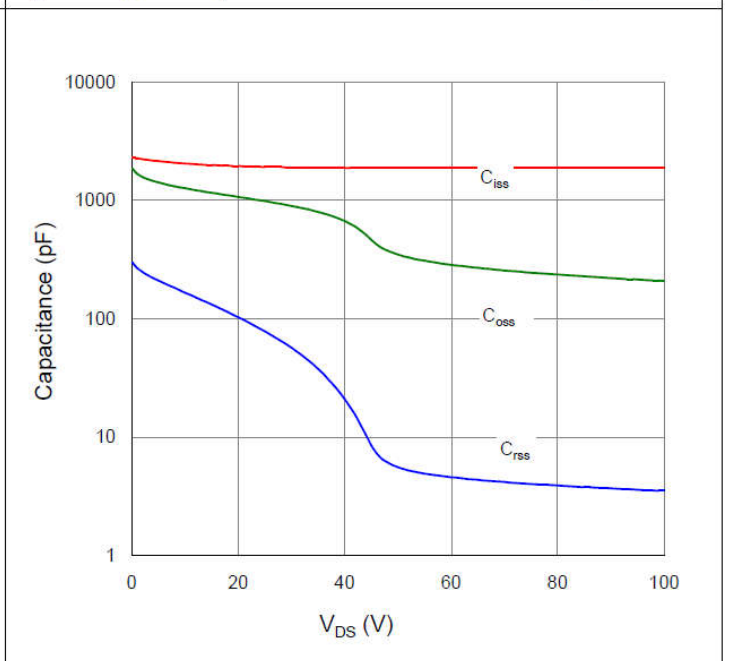


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage



Typical Operating Characteristics (Cont.)

Figure 9. Maximum Safe Operating Area

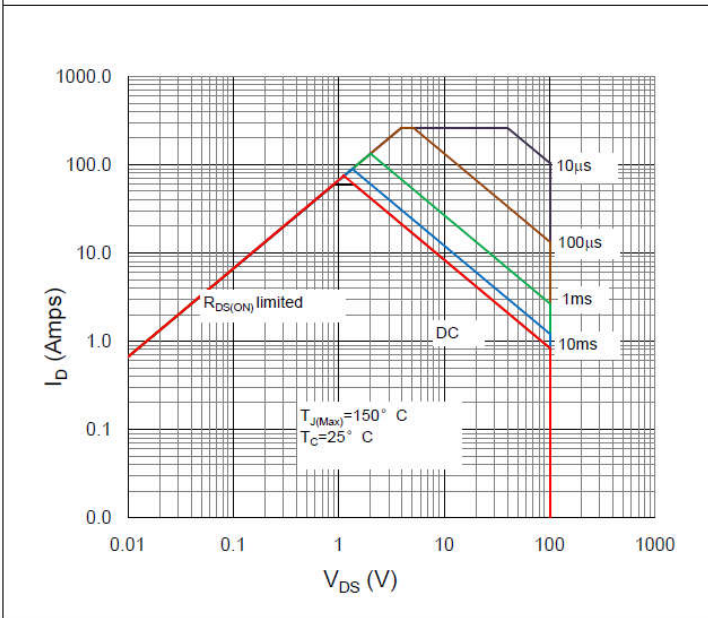


Figure 10. Maximum Drain Current vs. Case Temperature

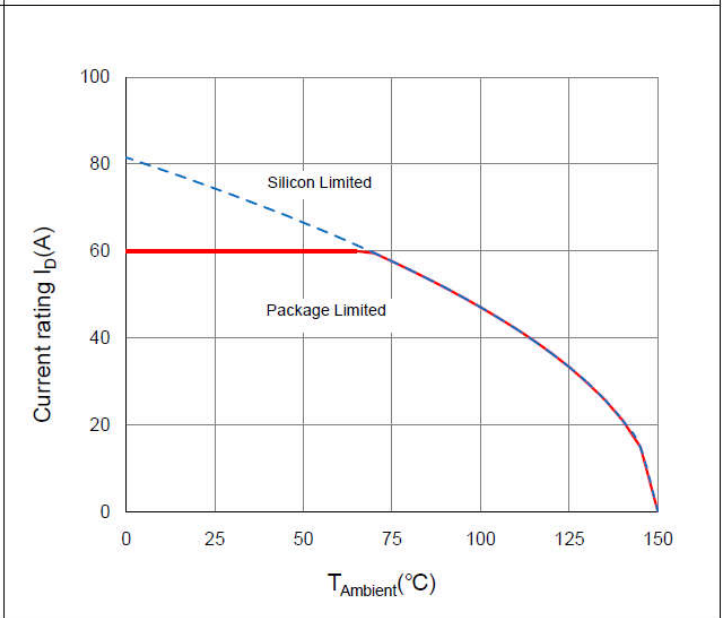
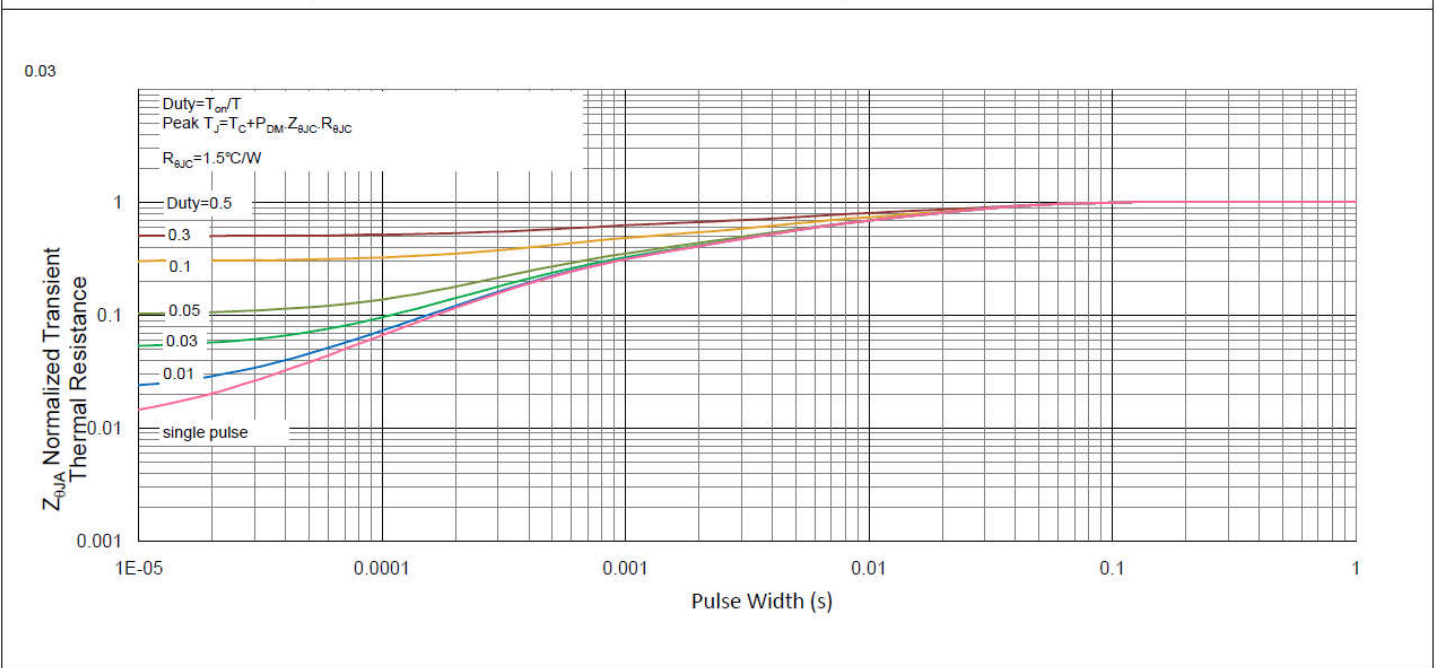


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



Design Notes